**LESSON PLAN**

**Subject Code & Name: VLSI TD**

**Branch: VLSI Class / Semester: IM.Tech-SEM 1 Academic Year:2015-16**

**Faculty: J.Swathi**

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| **Period** | **Date (Tentative)** | **Topic** | **Unit No.** | **Teaching Methodology** | **Remarks** | **Corrective action upon review** |
|  |  | **REVIEW OF MICROELECTRONICS & INTRODUCTION** | **I** |  |  |  |
| 1 | 23-9-15 | Introduction |  | BB |  |  |
| 2 | 24-9-15 | Technology trends and projections |  | BB |  |  |
| 3 | 25-9-15 | Lithography,oxidation,diffusion metallisation |  | BB |  |  |
| 4 | 28-9 | Fabrication process of PMOS and NMOS |  | BB |  |  |
| 5 | 30-9 | Fabrication process of CMOS and BiCMOS |  | BB |  |  |
| 6 | 1-10 | Basic electrical properties of MOS circuits Ids vs Vds relationship |  | BB |  |  |
| 7 | 5-10 | MOS,CMOS,BICMOS Inverters,Pass tr |  | BB |  |  |
| 8 | 7-10 | Zpu/Zpd ratios both 4:1 & 8:1 |  | BB |  |  |
| 9 | 8-10 | latchup in CMOS circuits |  | BB |  |  |
|  |  | **LAYOUT DESIGN AND TOOLS** | **II** |  |  |  |
| 10 | 9-10 | Introduction, Transistor structures, wires and vias |  | BB |  |  |
| 11 | 12-10 | Scalable design rules, lambda based design rules, stick diagrams |  | BB |  |  |
| 12 | 14-10 | Layout diagrams |  | BB |  |  |
| 13 | 15-10 | Logic gates: static complementary gates |  | BB |  |  |
| 14 | 19-10 | Delay analysis ,power optimization |  | BB |  |  |
| 15 | 26-10 | Switch logic, alternative gate circuits |  | BB |  |  |
| 16 | 28-10 | Low power gates |  | BB |  |  |
| 17 | 29-10 | RLC tx lines ,interconnect delays |  | BB |  |  |
|  |  | **COMBINATIONAL LOGIC NETWORKS** | **III** |  |  |  |
| 18 | 30-10 | Introduction, std. cell |  | BB |  |  |
| 19 | 3-11 | Structure, left edge algorithm |  | BB |  |  |
| 20 | 4-11 | Simulation, network delay |  | BB |  |  |
| 21 | 5-11 | Interconnect design |  |  |  |  |
| 22 | 6-11 | Power optimization & analysis |  |  |  |  |
| 23 | 10-11 | Switch logic networks |  | BB |  |  |
| 24 | 11-11 | Gate and network testing |  | BB |  |  |
| 25 | 12-11 | Combinational logic testing |  | BB |  |  |
|  |  | **SEQUENTIAL LOGIC NETWORKS** | **IV** |  |  |  |
| 26 | 13-11 | Introduction |  | BB |  |  |
| 27 | 23-11 | Memory cells and arrays |  | BB |  |  |
| 28 | 25-11 | Clocking disciplines |  | BB |  |  |
| 29 | 26-11 | System design of sequential circuits |  | BB |  |  |
| 30 | 27-11 | Power optimization & analysis |  | BB |  |  |
| 31 | 30-11 | Design and validation |  | BB |  |  |
| 32 | 2-12 | Testing of sequential machines |  | BB |  |  |
|  |  | **FLOORPLANNING** | **V** |  |  |  |
| 33 | 3-12 | Floor planning introduction |  | BB |  |  |
| 34 | 4-12 | Floor planning methods |  | BB |  |  |
| 35 | 7-12 | Off-chip connections |  |  |  |  |
| 36 | 9-12 | High level synthesis |  | BB |  |  |
| 37 | 10-12 | Architecture for low power SOCs |  | BB |  |  |
| 38 | 11-12 | CPUs |  |  |  |  |
| 39 | 14-12 | Embedded CPUs |  | BB |  |  |
| 40 | 16-12 | Architecture testing |  | BB |  |  |
| 41 | 17-12 | Validation |  | BB |  |  |
|  |  | **INTRODUCTION TO CAD SYSTEMS AND CHIP DESIGN** | **VI** |  |  |  |
| 42 | 18-12 | Introduction |  | BB |  |  |
| 43 | 19-12 | Chip design |  | BB |  |  |
| 44 | 21-12 | Layout synthesis |  | BB |  |  |
| 45 | 23-12 | Layout analysis |  | BB |  |  |
| 46 | 24-12 | Scheduling and printing |  | BB |  |  |
| 47 | 26-12 | Hardware/Software Co-design |  | BB |  |  |
| 48 | 28-12 | Chip-Design methodologies |  | BB |  |  |
| 49 | 4-12 | Chip-design IBM-ASIC Example |  | BB |  |  |
| 50 | 06-12 | Kitchen-Timer Chip |  | BB |  |  |
|  |  | Design of Kitchen -Timer chip |  | BB |  |  |

**CR: CLASS ROOM PPT: POWER POINT PRESENTATION LCD**

**Text books:**

1. Essentials of VLSI circuits and systems – Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005.
2. Principles of CMOS VLSI Design – Weste and Eshraghian, Pearson Education, 1999.

**Reference books:**

1. VLSI Design – Debaprasad Das, Oxford university press, 2010.
2. VLSI Design – A.Albert Raj and T.Latha, PHI Learing private limited 2010.
3. ASIC design - Smith.

**FACULTY HEAD OF THE DEPARTMENT**